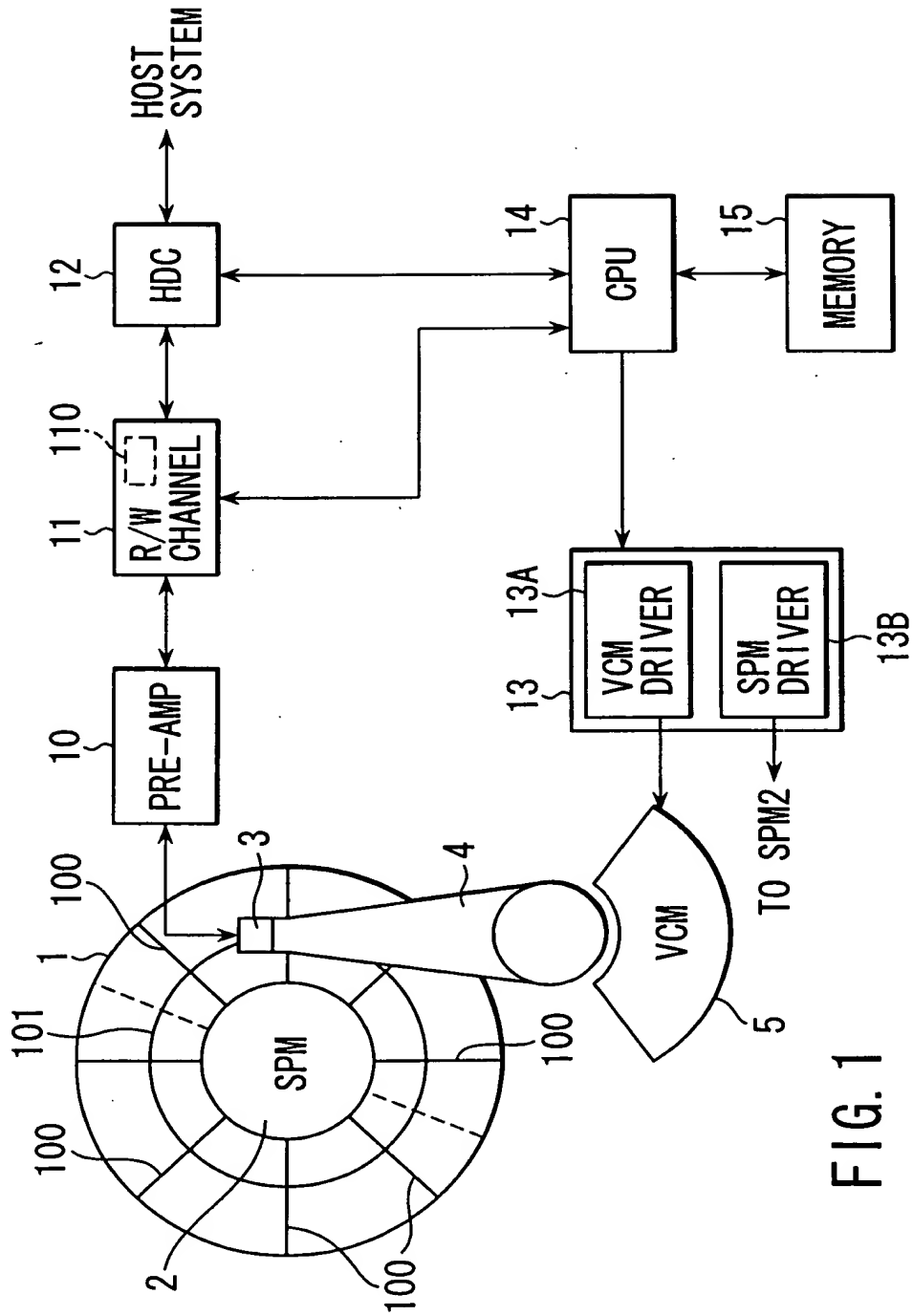
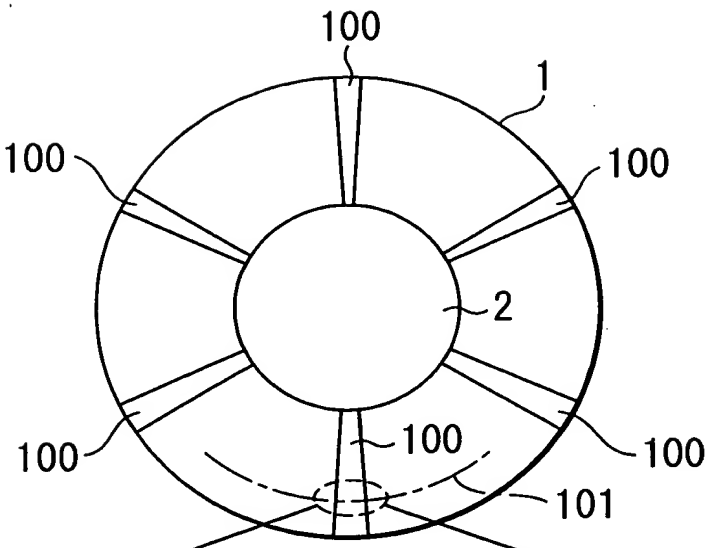

HOST SYSTEM
HDC
12
CPU
14
MEMORY
15
R/W CHANNEL
11
110
PRE-AMP
10
VCM DRIVER
13A
13
SPM DRIVER
13B
TO SPM2
VCM
5
SPM
1
2
3
4
100
101

FIG. 1

EDTS80: 1+2,2th60

FIG. 2A



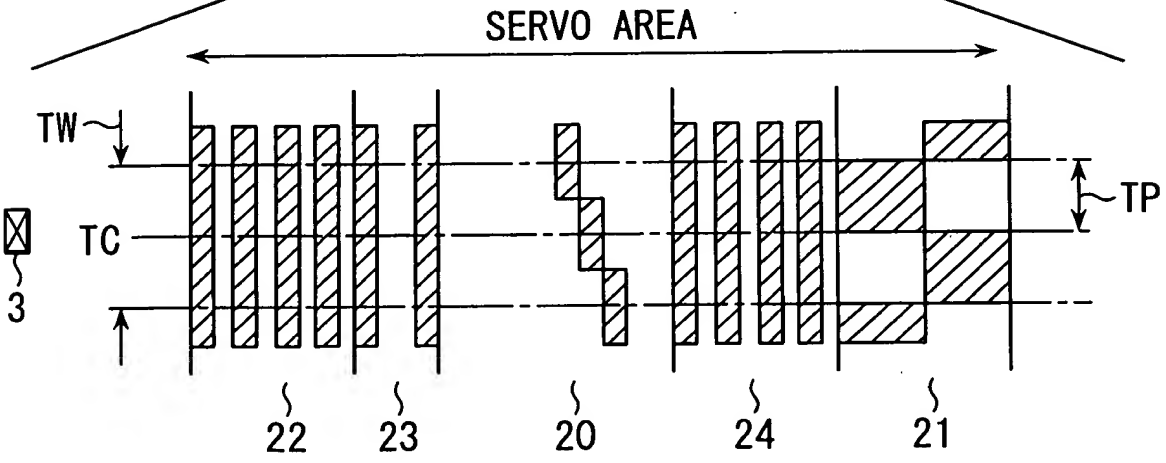


FIG. 2B

FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

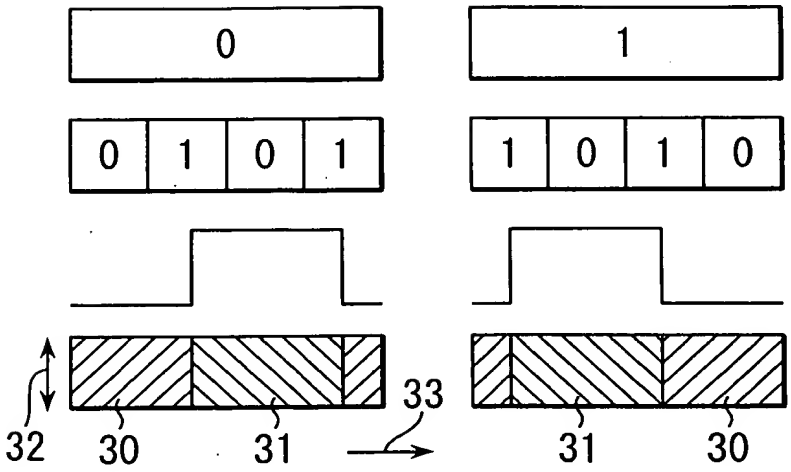


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

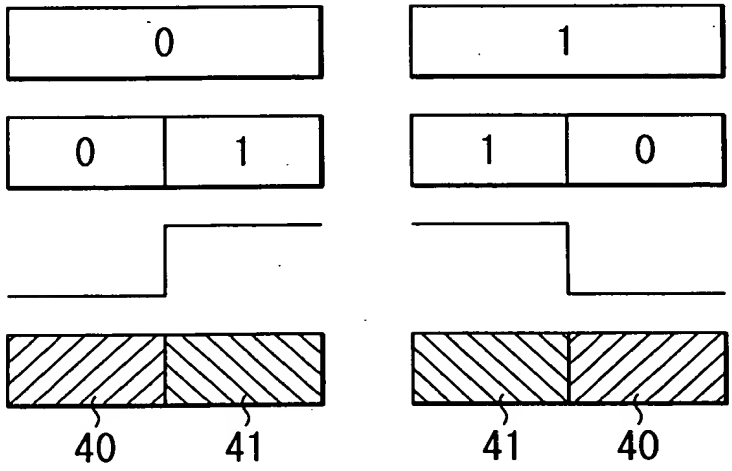
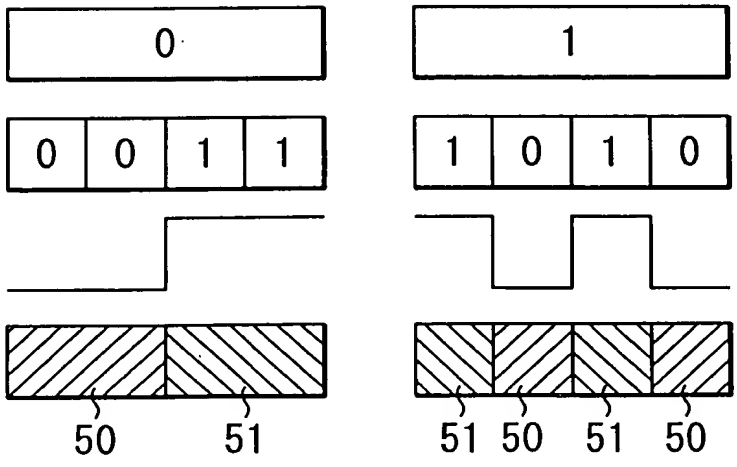


FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D



FOTE80 "T+7246960

TOTE80" Th∠2h660

FIG. 6A 1111000011001111

FIG. 6B 1010101010101010010101010101010110101010010101010101010101010

FIG. 6C -1 1 1-1-1 1 1-1-1 1 1-1-1 1 1-1-2-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1 0 1 1-1-1 1 1-1-2-1 1 1-1-1 1 1
-1-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1

FIG. 6D 1111111111111111101111111111111111101111111101111111
1111111111111111

FIG. 6E 1010101010101010010101010101010110101010010101010101010101010

FIG. 7A 1111

FIG. 7B 00001100

FIG. 7C 1111

FIG. 7D 1010 1010 1010 1010

FIG. 7E 0101 0101 0101 0101 1010 1010 0101 0101

FIG. 7F 1010 1010 1010 1010

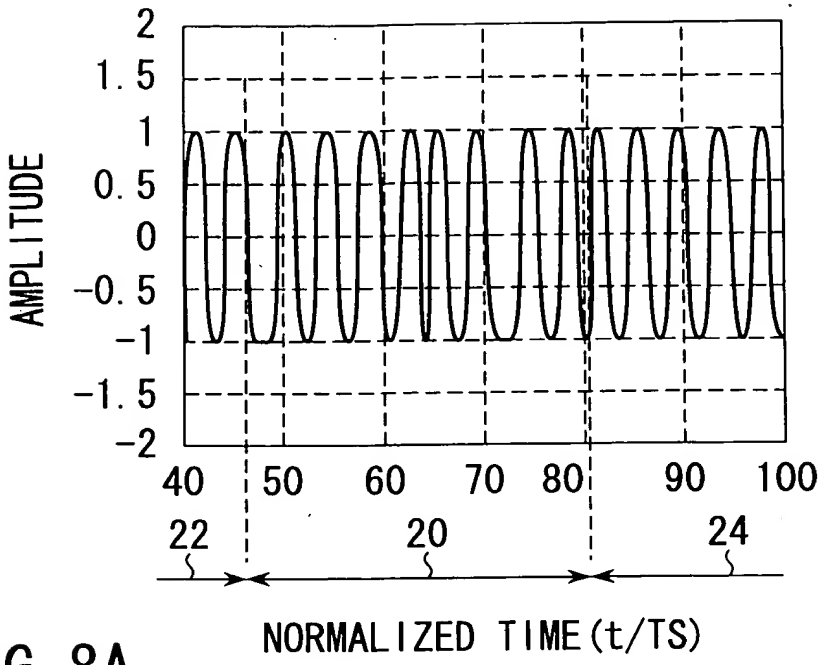

AMPLITUDE
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
40
50
60
70
80
90
100
22
20
24
NORMALIZED TIME(t/TS)

FIG. 8A

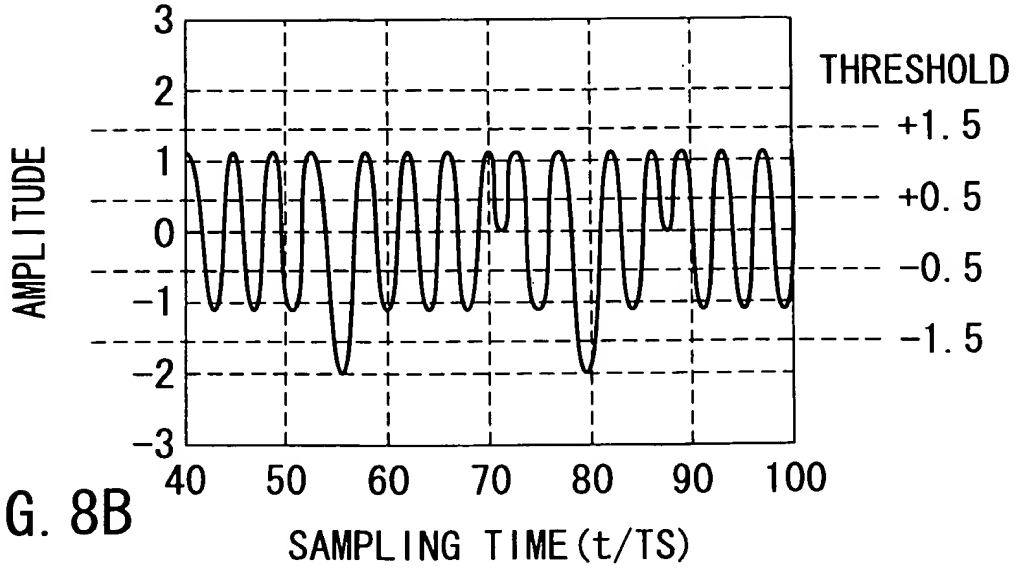

AMPLITUDE
3
2
1
0
-1
-2
-3
40
50
60
70
80
90
100
THRESHOLD
+1.5
+0.5
-0.5
-1.5
SAMPLING TIME(t/TS)

FIG. 8B

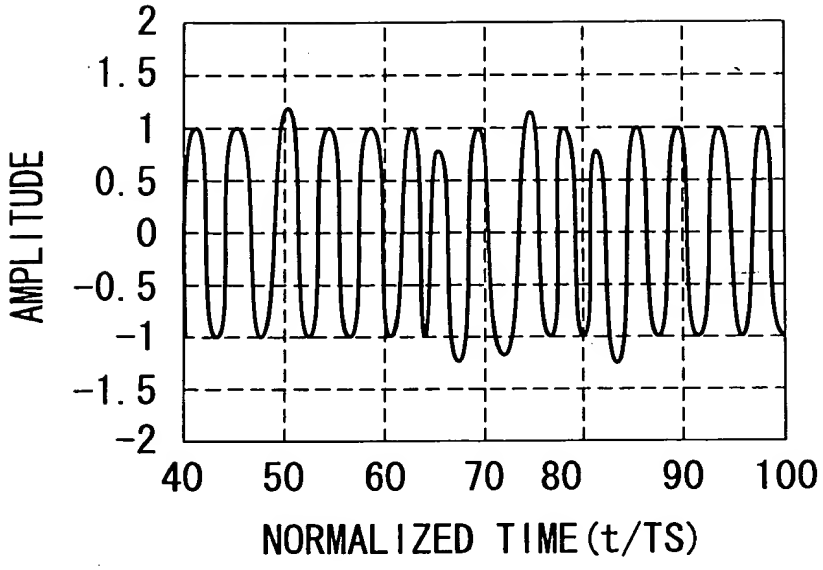

AMPLITUDE
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
40
50
60
70
80
90
100
NORMALIZED TIME(t/TS)

FIG. 9A

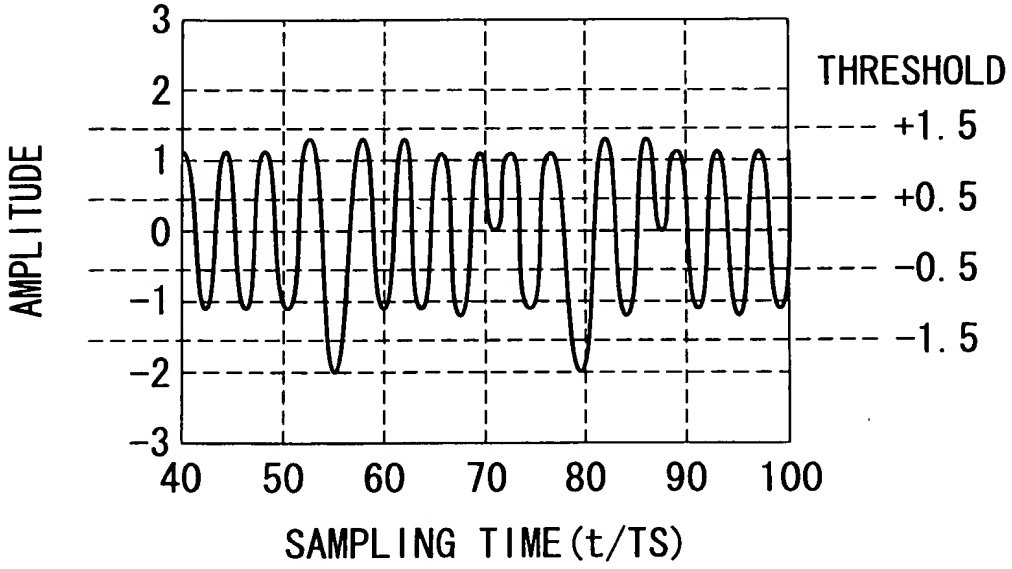

AMPLITUDE
3
2
1
0
-1
-2
-3
40
50
60
70
80
90
100
SAMPLING TIME(t/TS)
THRESHOLD
+1.5
+0.5
-0.5
-1.5

FIG. 9B

0	→	0000
1	→	1010

FIG. 10A

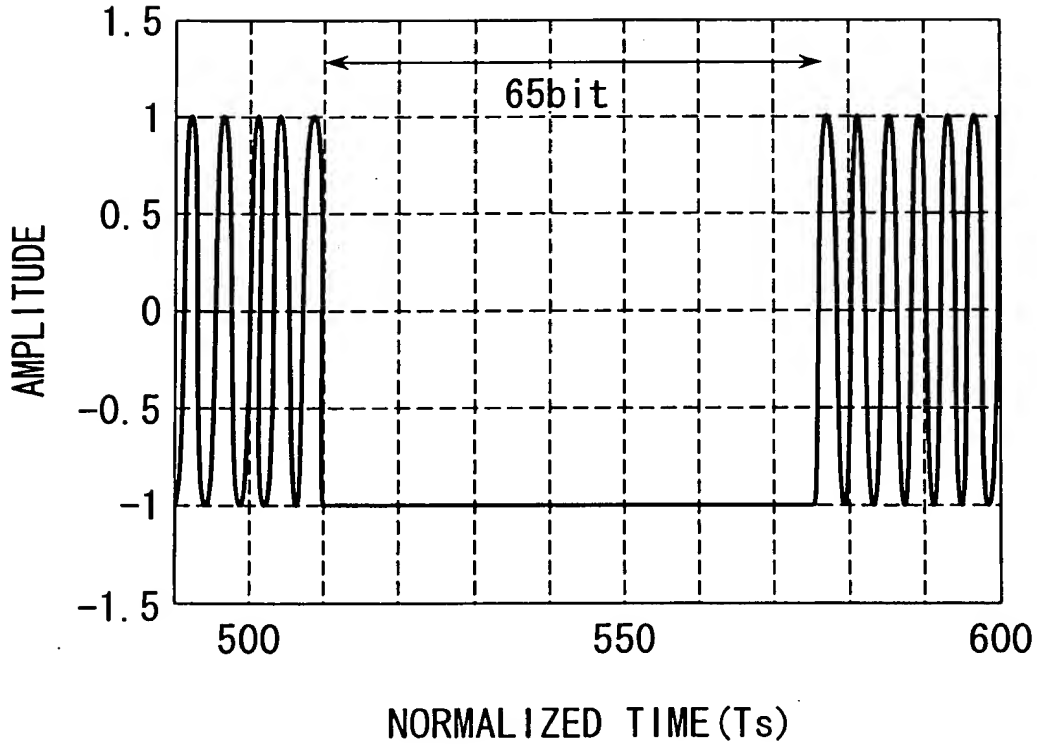


FIG. 10B

FOTE30: Tx/2h650

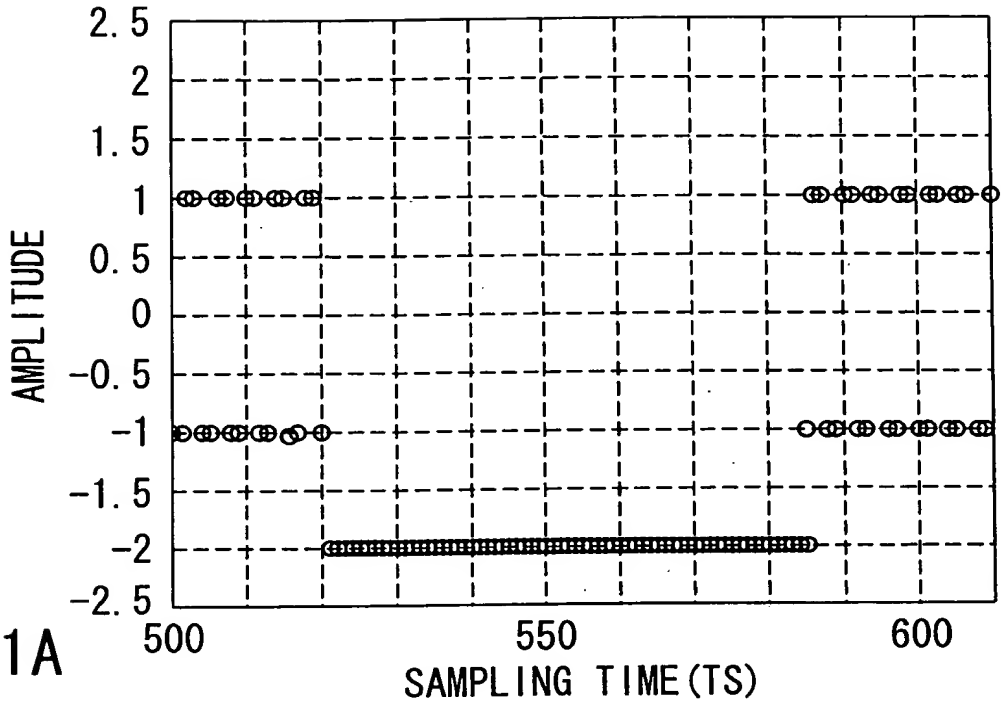


FIG. 11A

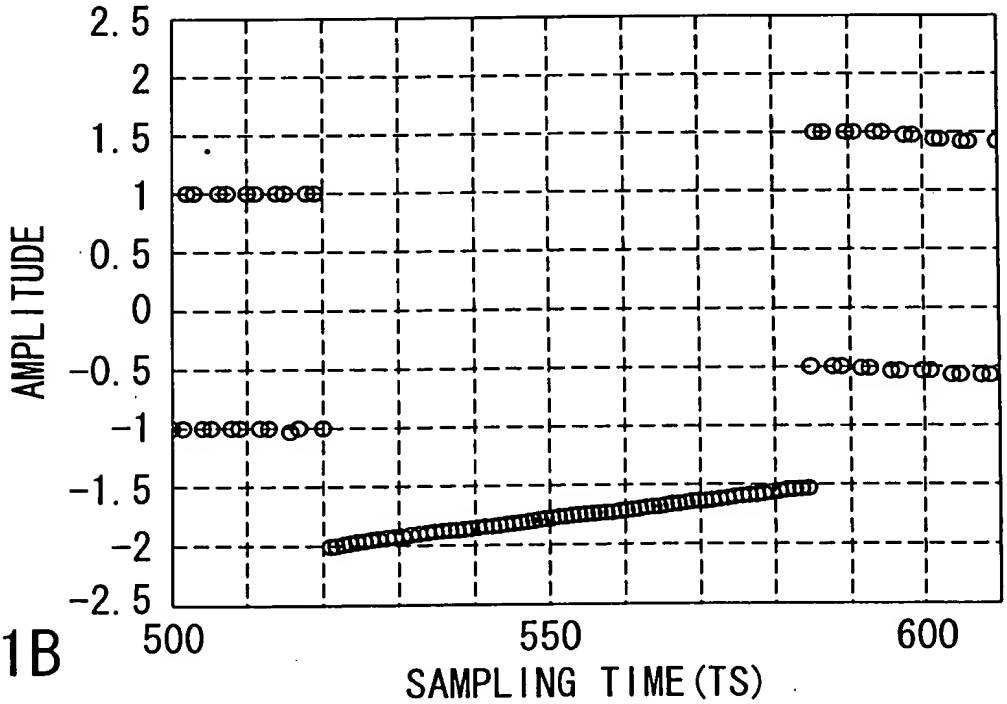


FIG. 11B

09945441 083101

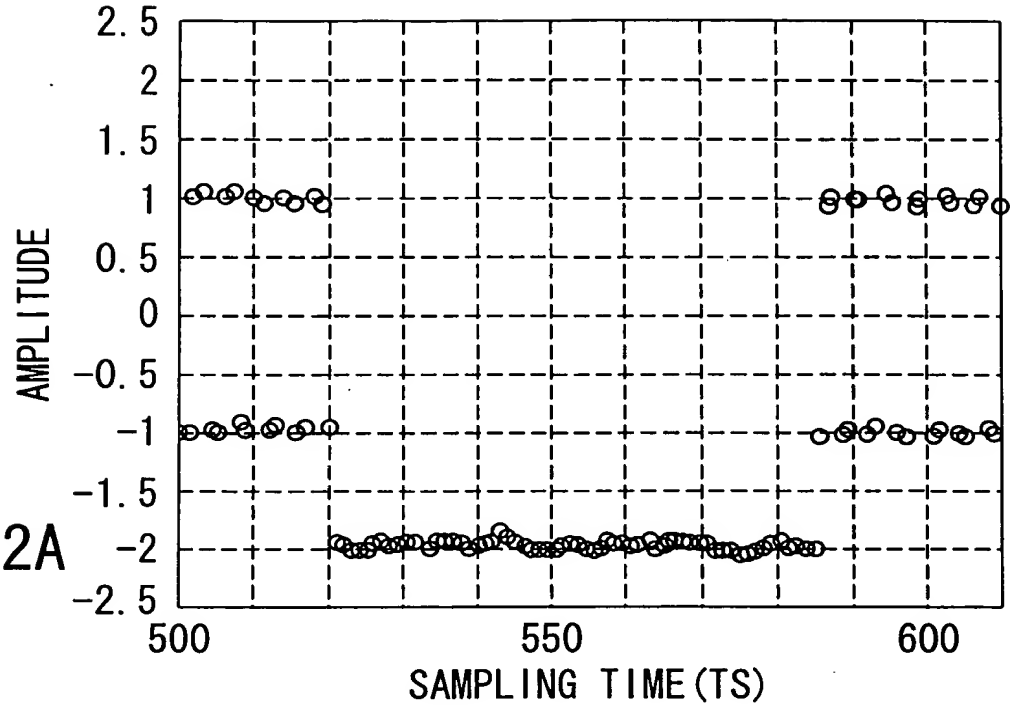


FIG. 12A

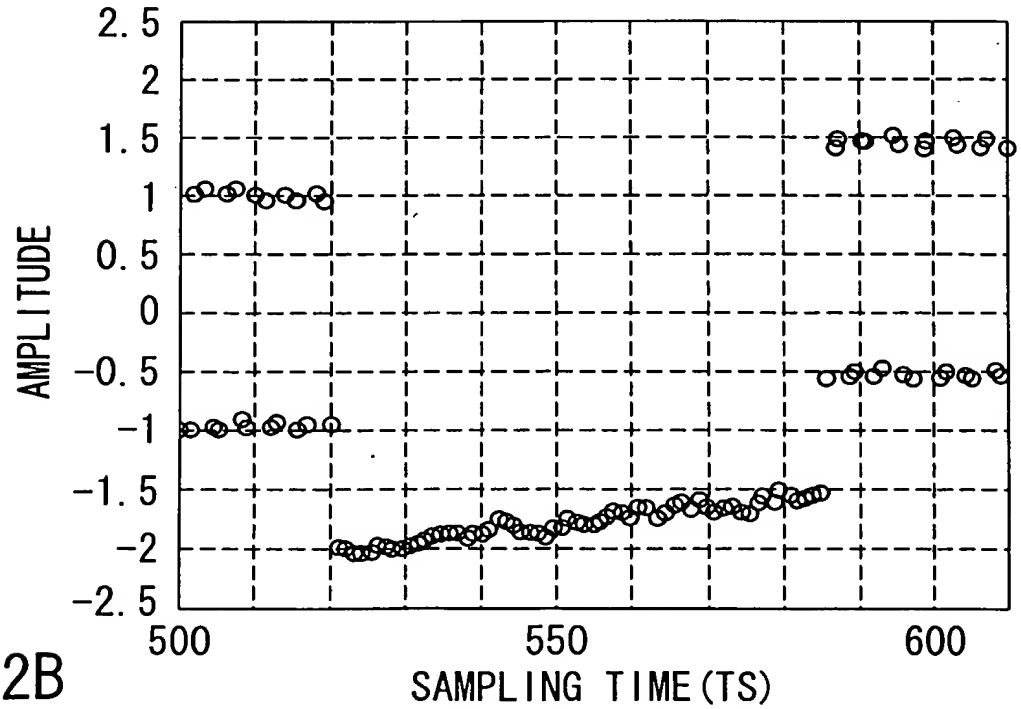


FIG. 12B

EP1359760 A1 20031105

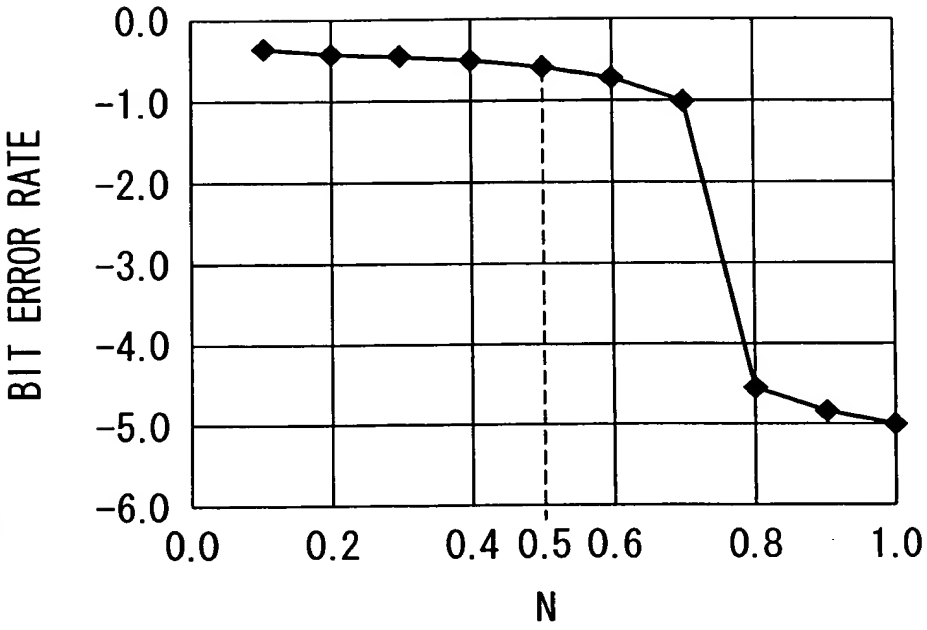


FIG. 13

	Tmin=65(bit)			
	N	$fc=\frac{-\ln N}{2\pi Tmin}$	BER	BER(log)
	0.1	5.64E-03	4.46E-01	-0.3506
	0.2	3.94E-03	4.09E-01	-0.3880
	0.3	2.95E-03	3.81E-01	-0.4192
	0.4	2.24E-03	3.44E-01	-0.4631
	0.5	1.70E-03	2.97E-01	-0.5272
	0.6	1.25E-03	2.26E-01	-0.6454
	0.7	8.73E-04	1.14E-01	-0.9419
	0.8	5.46E-04	2.93E-05	-4.5324
	0.9	2.58E-04	1.49E-05	-4.8268
	1.0	0.00E+00	1.10E-05	-4.9586

FIG. 14

FIG. 15A (PRIOR ART) 1111000011001111

FIG. 15B (PRIOR ART) 1010101010101010000000000000000010101010000000001010101010101010

FIG. 15C (PRIOR ART) -1 1 1-1-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1-2-2-2-2-2-2-2-2-2-2-2-2-2-2-2-2-1 1 1-1-1 1 1-1-2-2-2-2-2-2-2-2-2-1-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1-1-1 1 1

FIG. 15D (PRIOR ART) 1111111111111111000000000000000011111111000000001111111111111111

FIG. 15E (PRIOR ART) 1010101010101010000000000000000010101010000000001010101010101010

FIG. 18A (PRIOR ART) 1111

FIG. 18B (PRIOR ART) 00001100

FIG. 18C (PRIOR ART) 1111

FIG. 18D (PRIOR ART) 1010 1010 1010 1010

FIG. 18E (PRIOR ART) 0000 0000 0000 0000 1010 1010 0000 0000

FIG. 18F (PRIOR ART) 1010 1010 1010 1010

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FIG. 16A
(PRIOR ART)

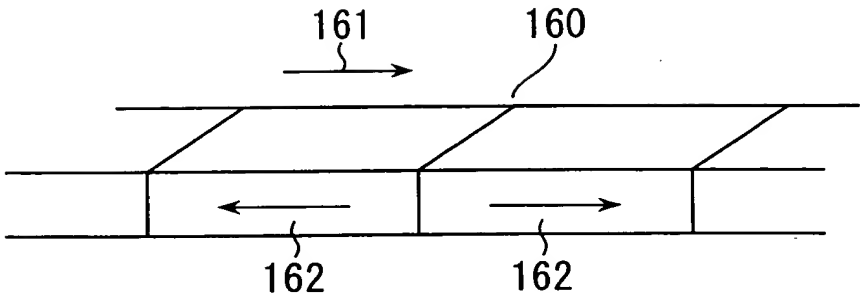


FIG. 16B
(PRIOR ART)

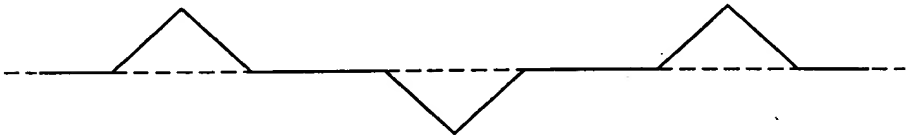


FIG. 17A
(PRIOR ART)

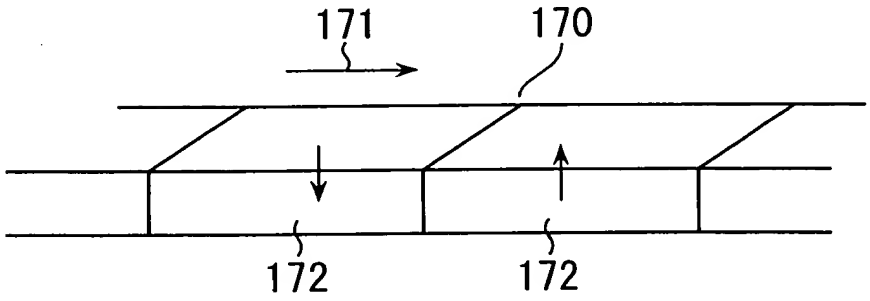
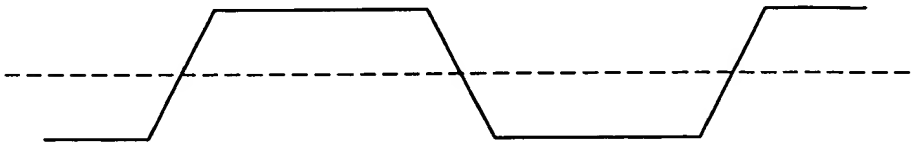


FIG. 17B
(PRIOR ART)



EP 1 276 660 A2

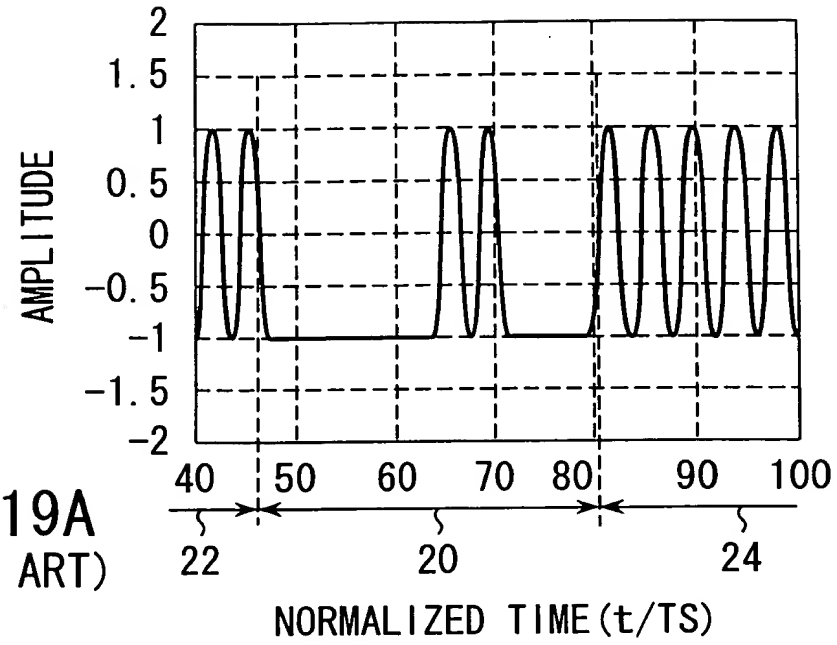


FIG. 19A
(PRIOR ART)

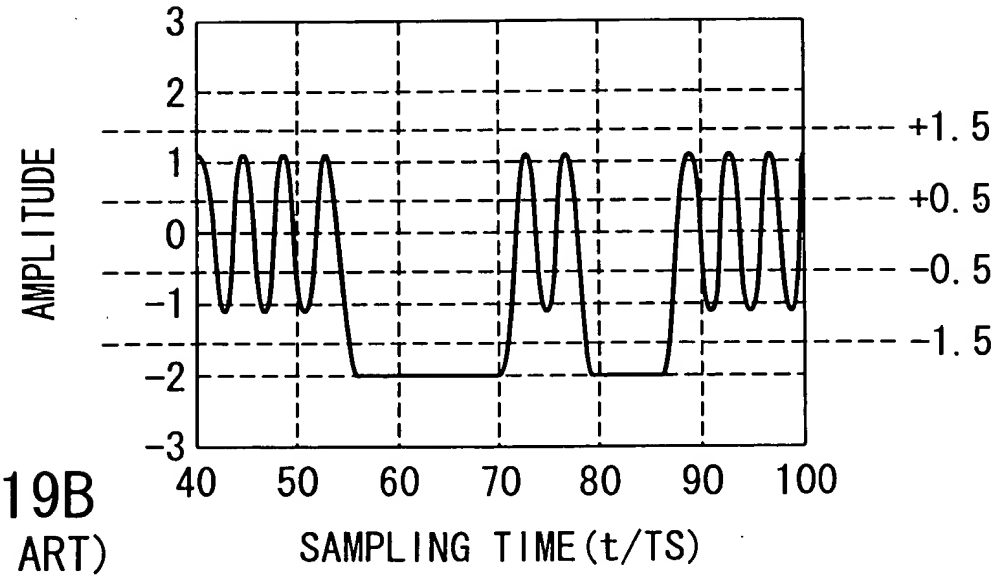


FIG. 19B
(PRIOR ART)

JP2002-247660

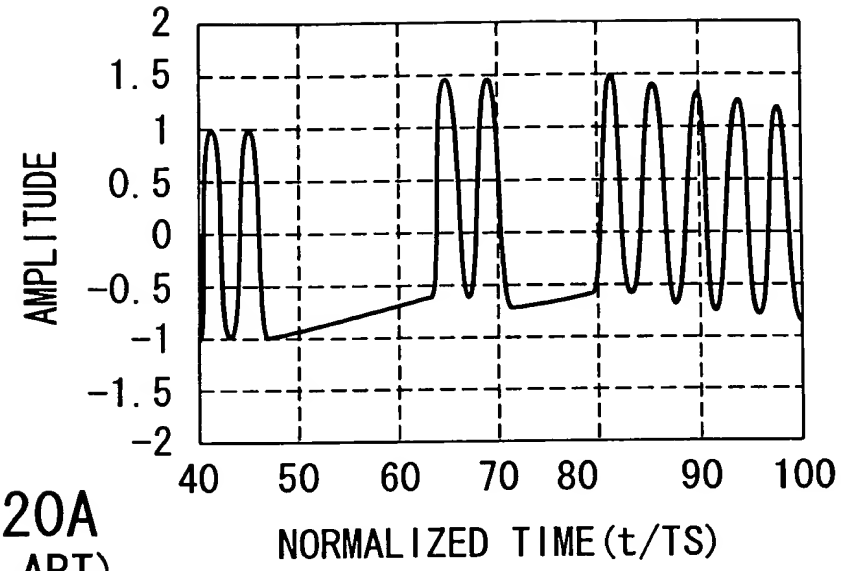


FIG. 20A
(PRIOR ART)

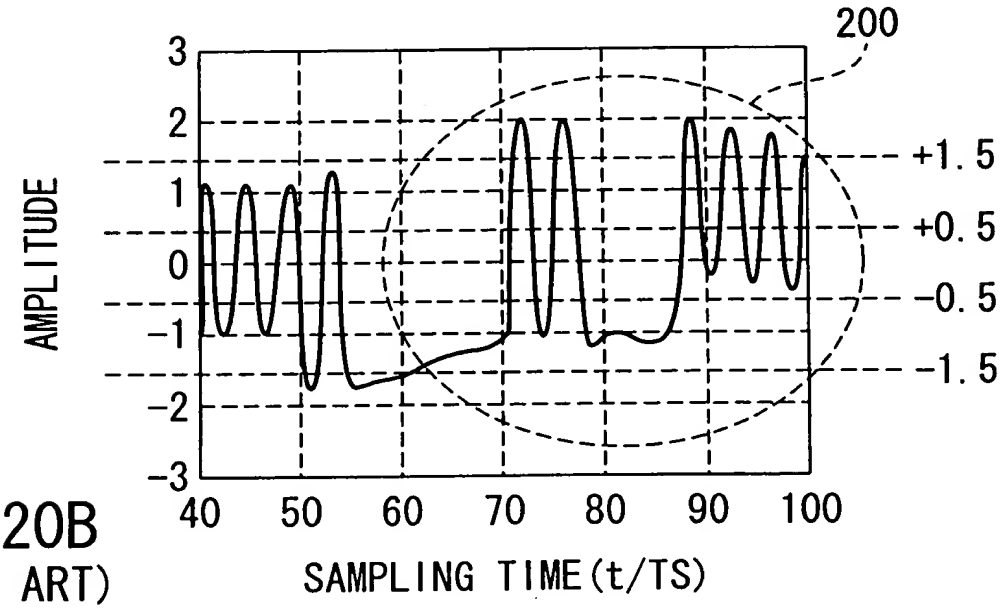


FIG. 20B
(PRIOR ART)